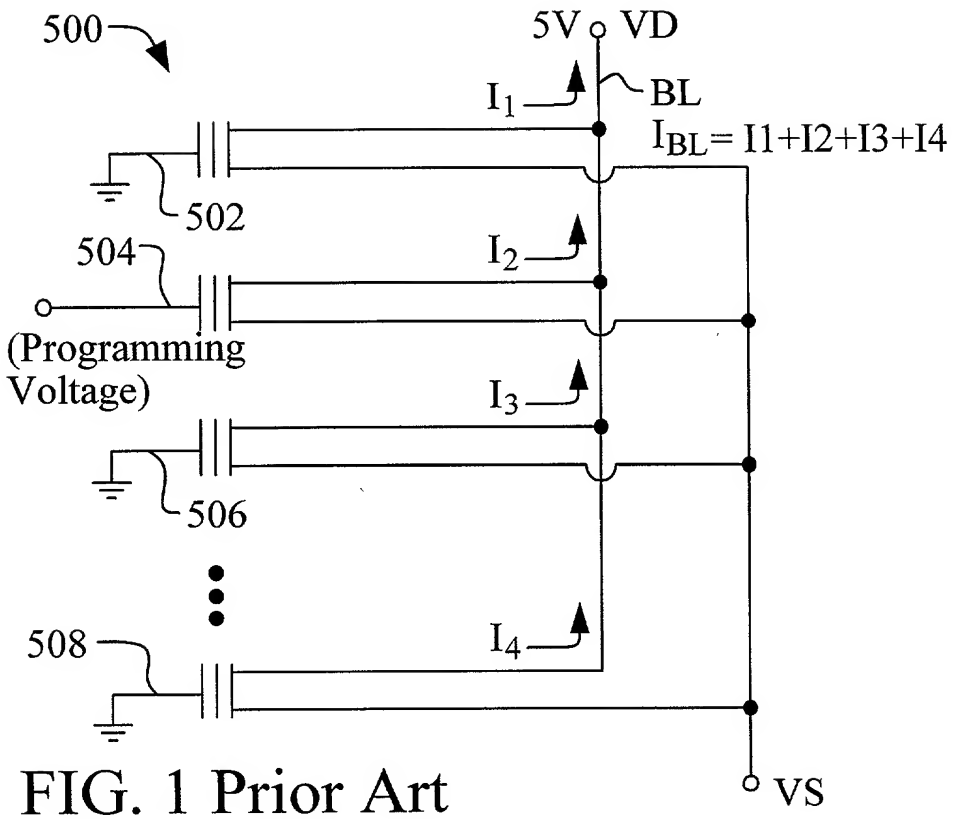

FIG. 1 Prior Art

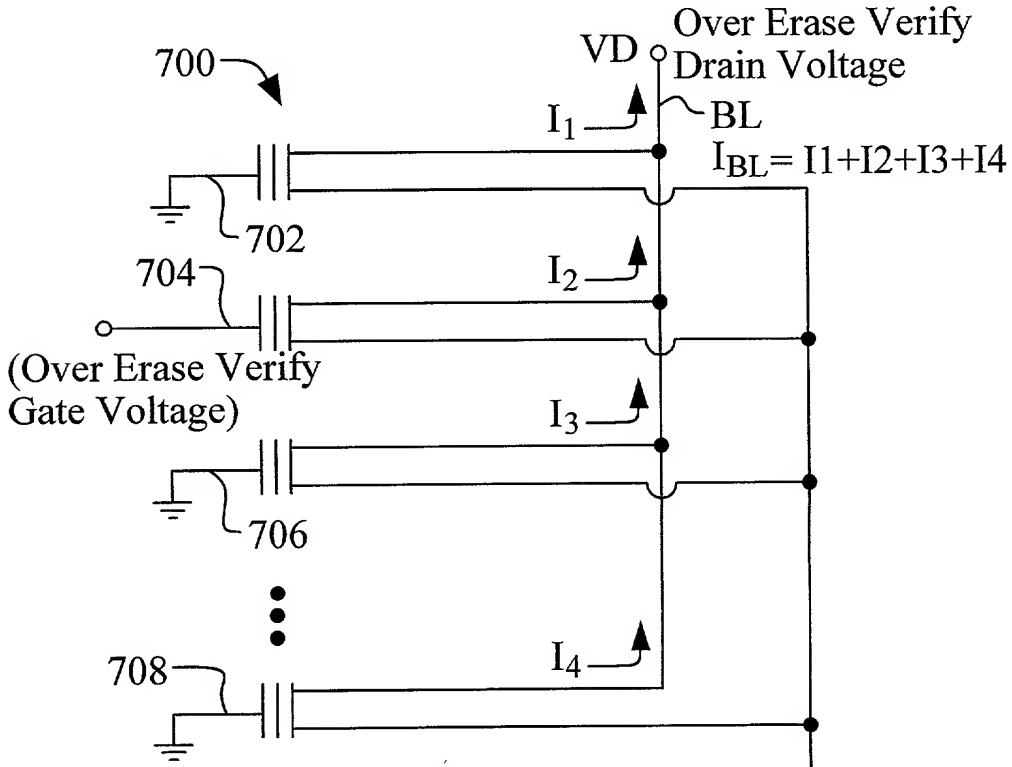

FIG. 2 Prior Art

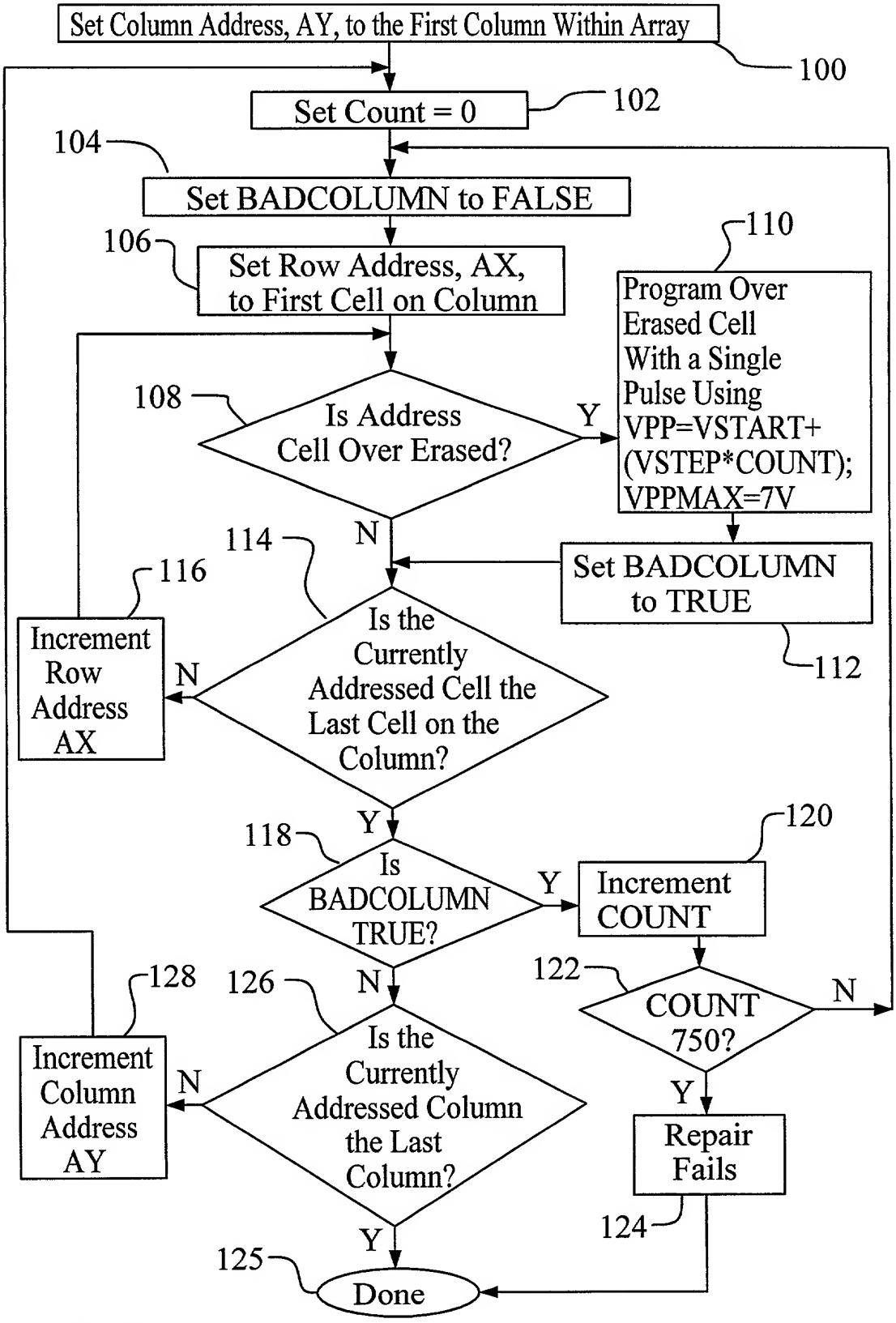

FIG. 3 Prior Art

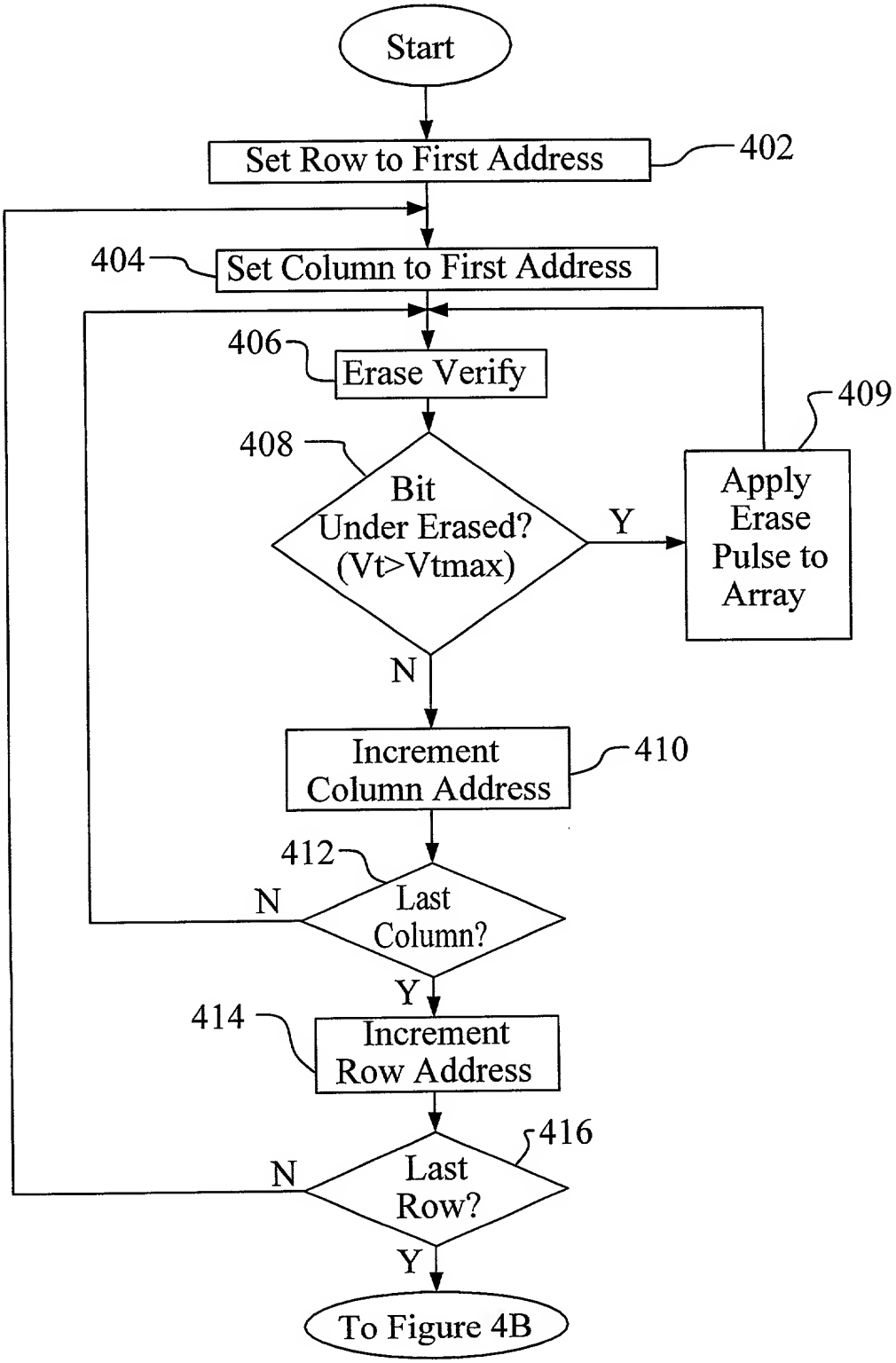

FIG. 4A Prior Art

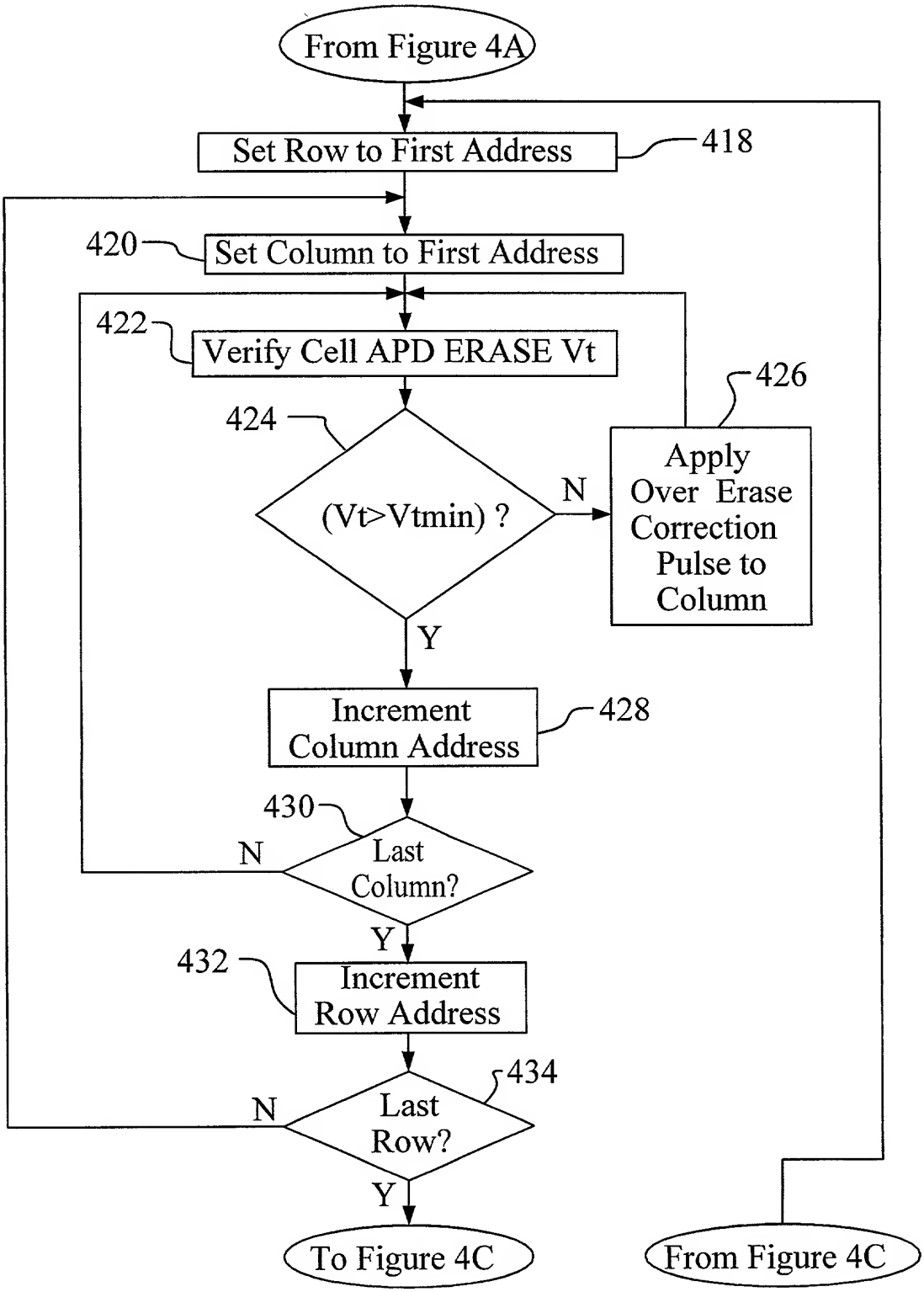

FIG. 4B Prior Art

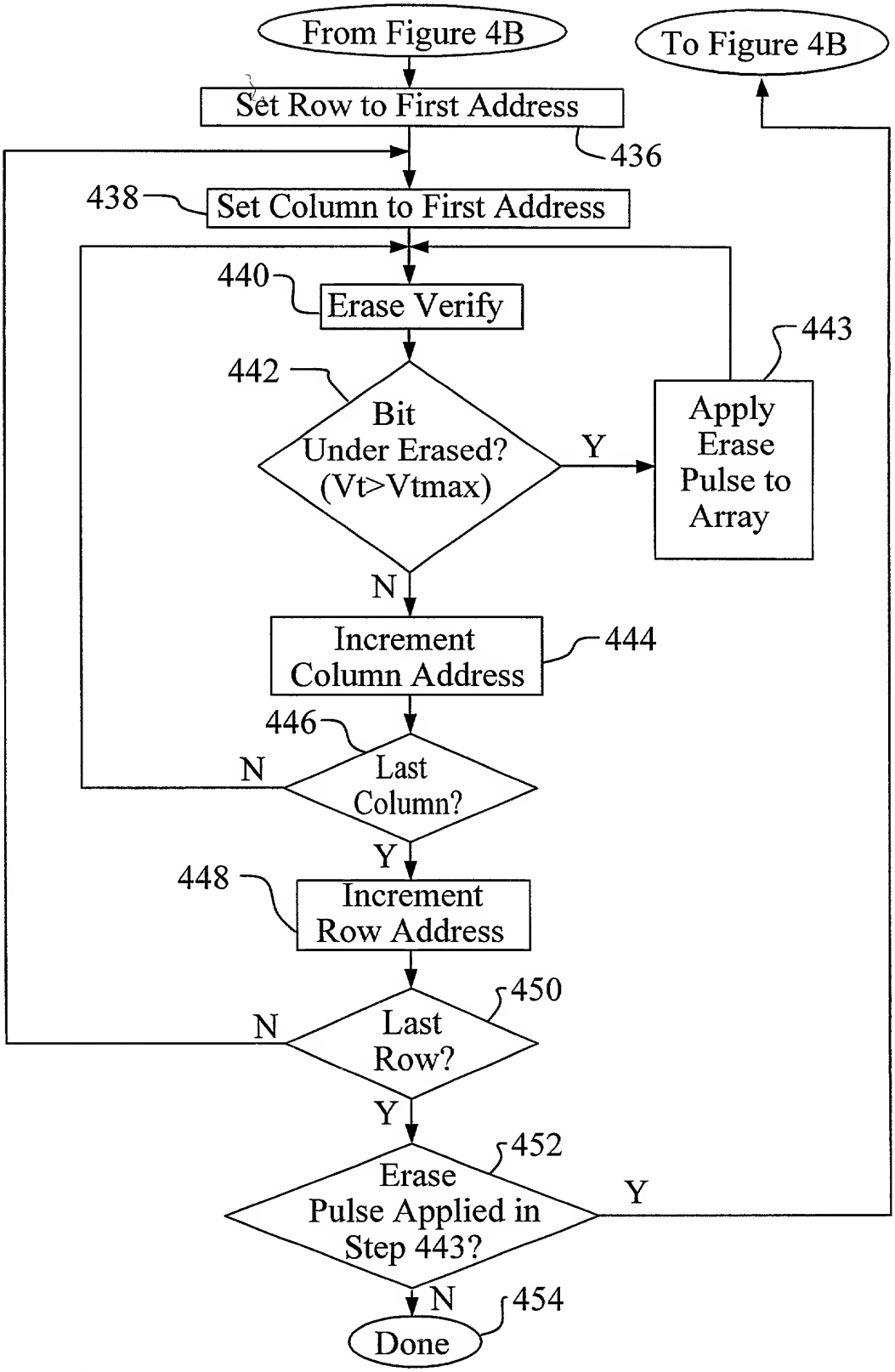

FIG. 4C Prior Art

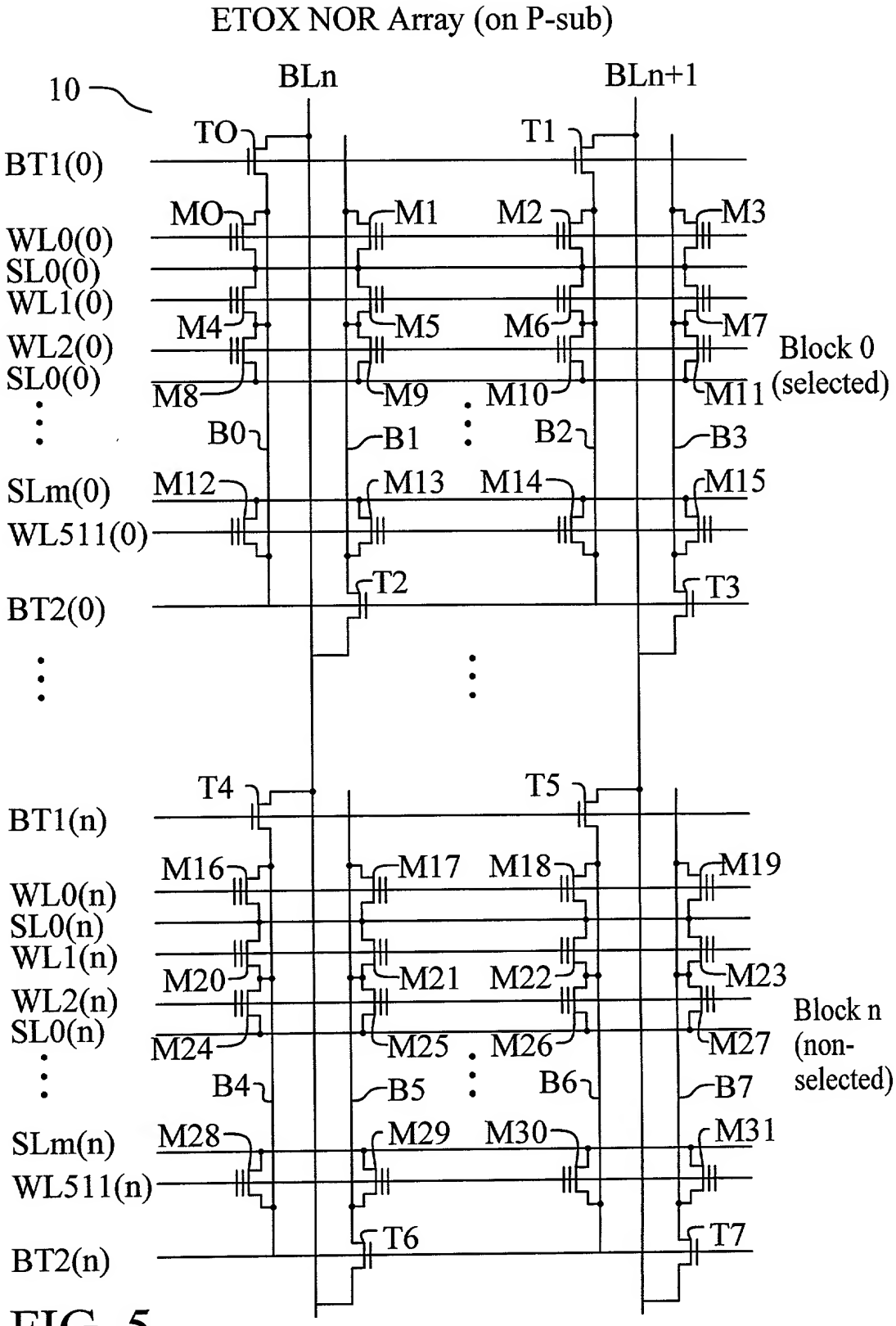
ETOX NOR Array (on P-sub)
10
BLn
BLn+1
TO
T1
BT1(0)
MO
M1
M2
M3
WL0(0)
SL0(0)
WL1(0)
M4
M5
M6
M7
WL2(0)
SL0(0)
Block 0
(selected)
M8
M9
M10
M11
B0
B1
B2
B3
SLm(0)
M12
M13
M14
M15
WL511(0)
T2
T3
BT2(0)
T4
T5
BT1(n)
M16
M17
M18
M19
WL0(n)
SL0(n)
WL1(n)
M20
M21
M22
M23
WL2(n)
SL0(n)
Block n
(non-
selected)
M24
M25
M26
M27
B4
B5
B6
B7
SLm(n)
M28
M29
M30
M31
WL511(n)
T6
T7
BT2(n)

FIG. 5

		Erase	Erase Verify*	Erase Inhibit**	Correction Verify***	Correction***
	BLn	0V	0V	0V	0V	0V
	BLn+1	0V	+1V	0V	+1V	+5V
Block 0 (selected)	BT1(0)	0V	0V	0V	0V	0V
	WL0(0)	-10V	Versvfy	-10V	0V	0V
	SL0(0)	+5V	0V	+5V	0V	0V
	WL1(0)	-10V	-4V	-10V	Vcorvfy	Vcorr
	WL2(0)	-10V	-4V	-10V	-4V	-4V
	SLm(0)	+5V	0V	0V	0V	0V
	WL511(0)	-10V	-4V	0V	-4V	-4V
	BT2(0)	0V	Vdd	0V	Vdd	+10V
Block n (non-selected)	BT1(n)	0V	0V	0V	0V	0V
	WL0(n)	0V	0V	0V	0V	0V
	SL0(n)	0V	0V	0V	0V	0V
	WL1(n)	0V	0V	0V	0V	0V
	WL2(n)	0V	0V	0V	0V	0V
	SLm(n)	0V	0V	0V	0V	0V
	WL511(n)	0V	0V	0V	0V	0V
	BT2(n)	0V	0V	0V	0V	0V

Note: * M3 is selected
** M12, M13, M14 and M15 are selected
*** M7 is selected; M0, M1, M2 and M3 pass the verification of correction

FIG. 6

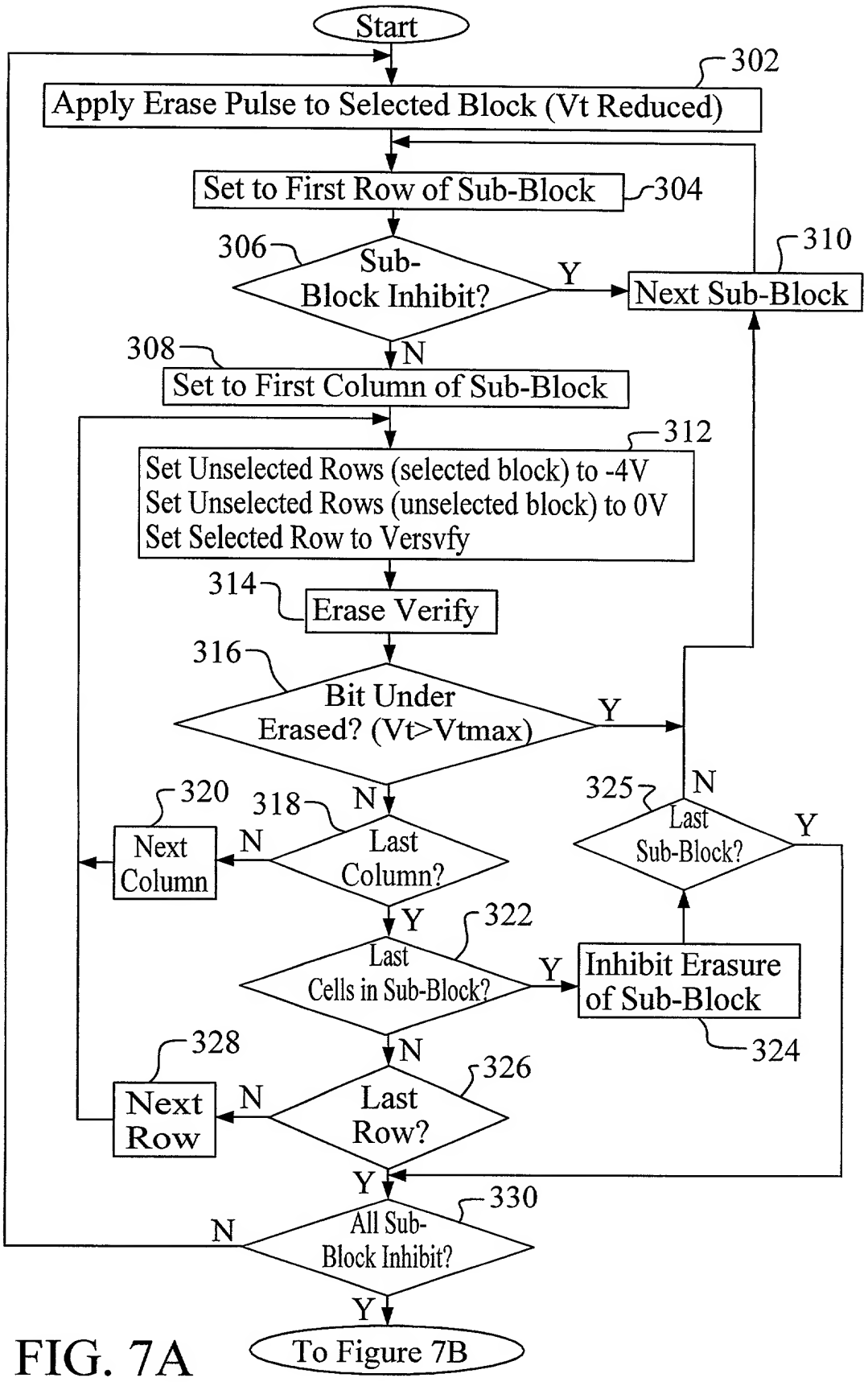
Start
302
Apply Erase Pulse to Selected Block (Vt Reduced)
Set to First Row of Sub-Block
304
306
Sub-Block Inhibit?
Y
310
Next Sub-Block
N
308
Set to First Column of Sub-Block
312
Set Unselected Rows (selected block) to -4V
Set Unselected Rows (unselected block) to 0V
Set Selected Row to Versvfy
314
Erase Verify
316
Bit Under Erased? (Vt>Vtmax)
Y
N
320
318
Next Column
N
Last Column?
325
N
Last Sub-Block?
Y
Y
322
Last Cells in Sub-Block?
Y
Inhibit Erasure of Sub-Block
324
N
328
326
Next Row
N
Last Row?
Y
330
N
All Sub-Block Inhibit?
Y
To Figure 7B

FIG. 7A

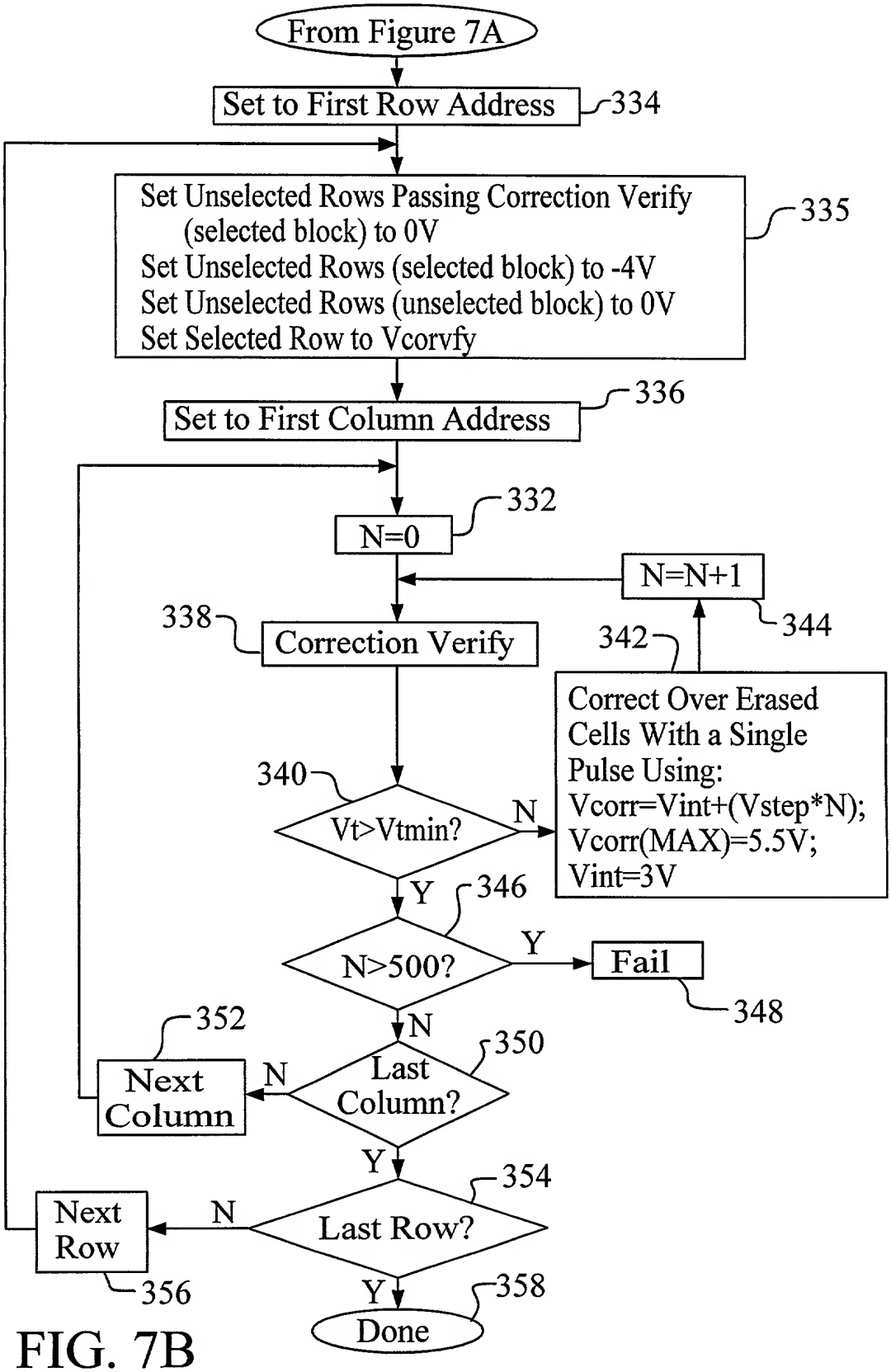
From Figure 7A
Set to First Row Address
334
Set Unselected Rows Passing Correction Verify (selected block) to 0V
Set Unselected Rows (selected block) to -4V
Set Unselected Rows (unselected block) to 0V
Set Selected Row to Vcorvfy
335
Set to First Column Address
336
N=0
332
N=N+1
344
338
Correction Verify
342
Correct Over Erased Cells With a Single Pulse Using:
Vcorr=Vint+(Vstep*N);
Vcorr(MAX)=5.5V;
Vint=3V
340
Vt>Vtmin?
N
Y
346
N>500?
Y
Fail
348
N
352
Next Column
N
350
Last Column?
Y
354
Next Row
N
Last Row?
356
Y
358
Done

FIG. 7B

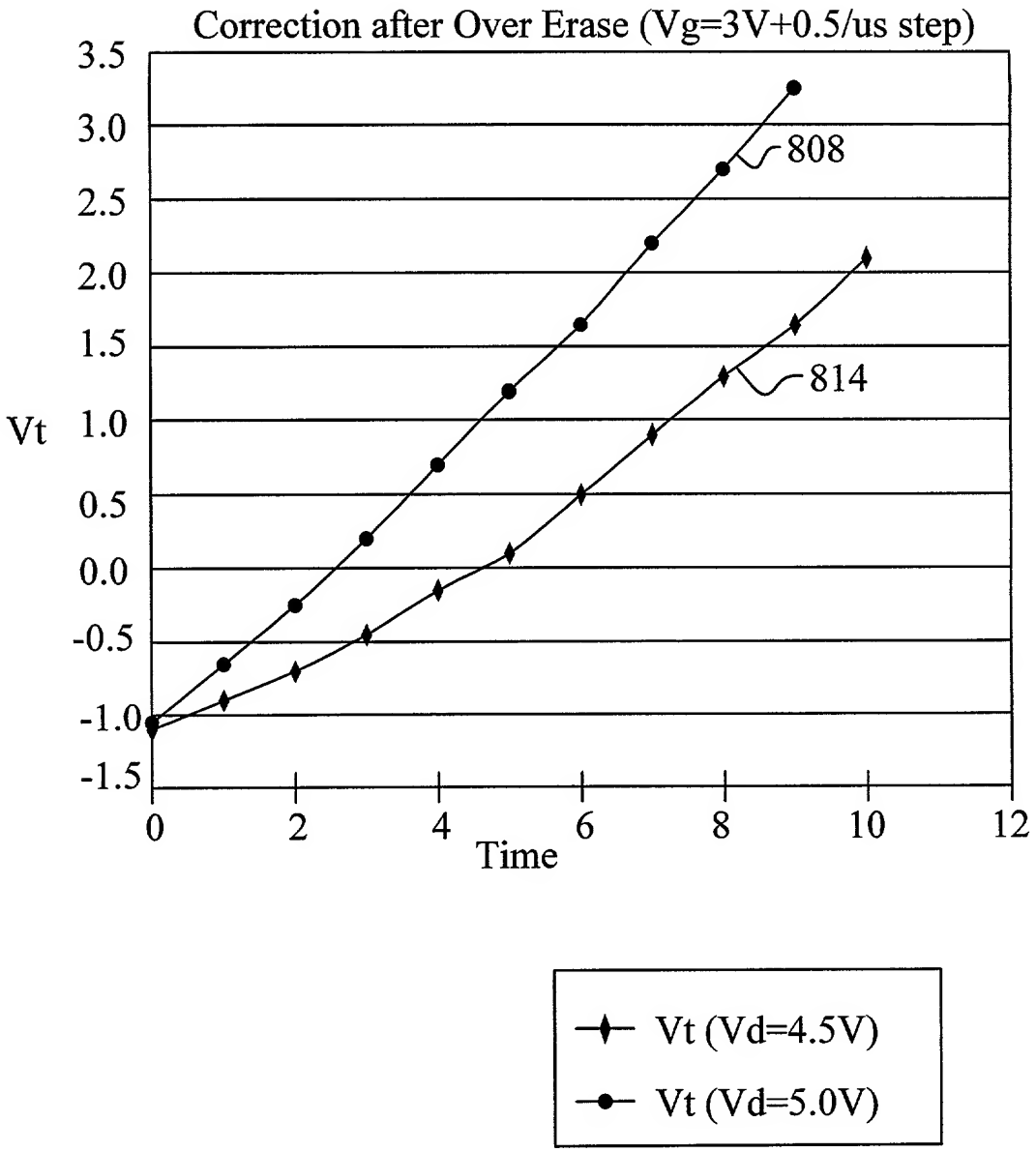
Correction after Over Erase (Vg=3V+0.5/us step)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
Vt
0
2
4
6
8
10
12
Time
808
814
Vt (Vd=4.5V)
Vt (Vd=5.0V)

FIG. 8

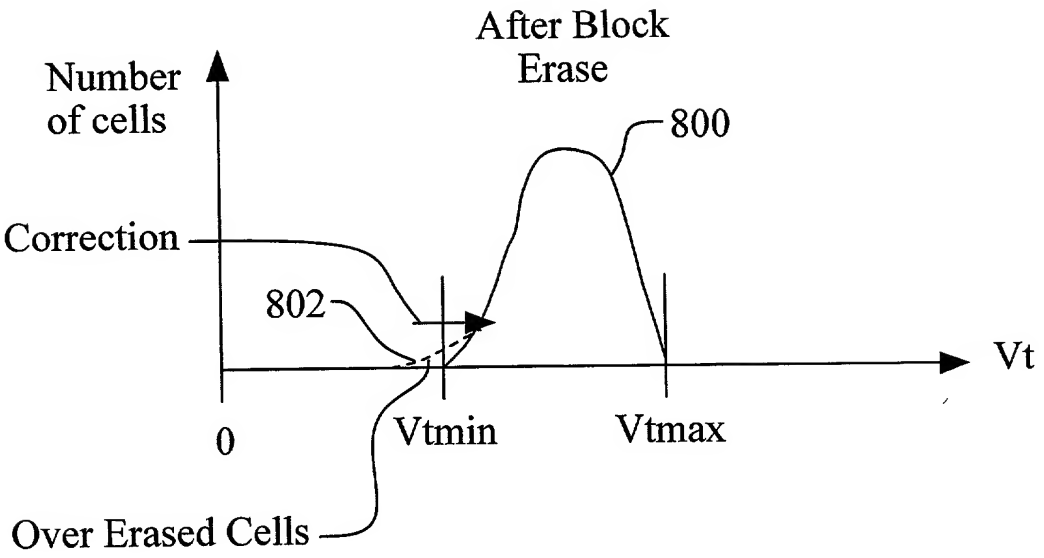

FIG. 9A Prior Art

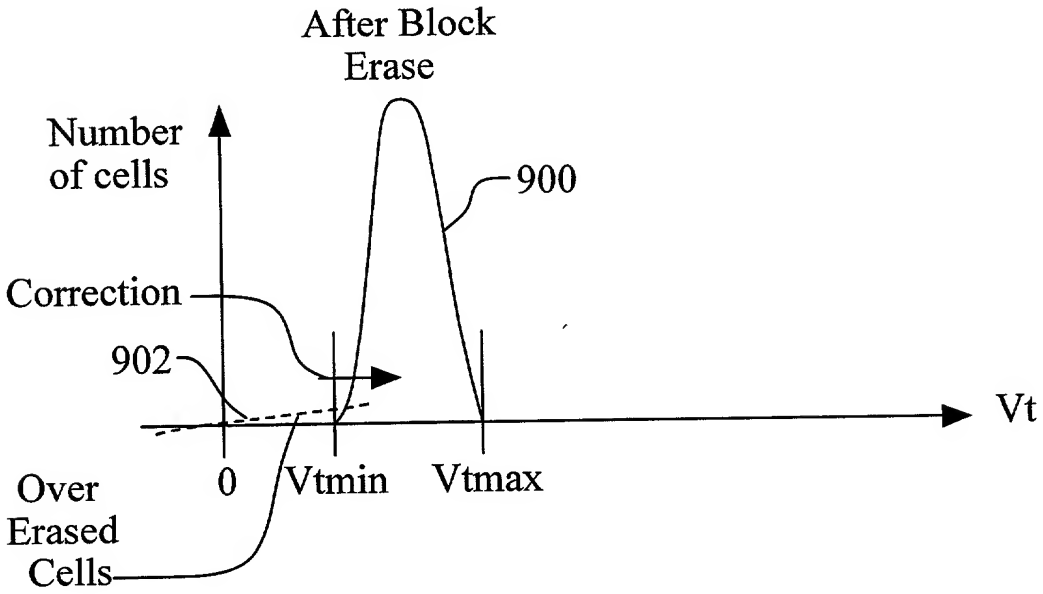

FIG. 9B

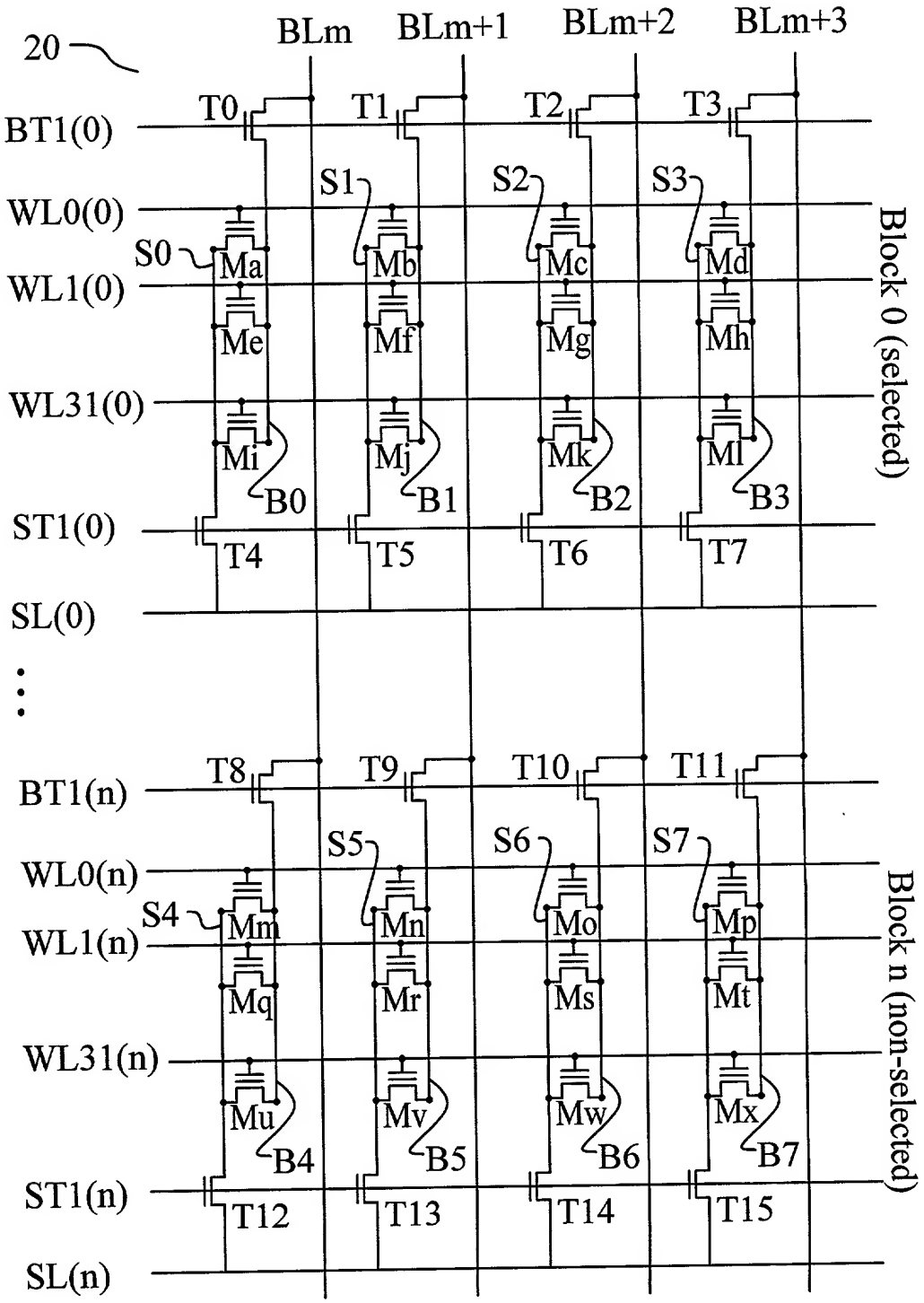

FIG. 10 Prior Art

		Erase	Erase Verify*	Erase Inhibit**	Correction Verify*	Correction***
	BLm	0V	+1V	0V	+1V	0V
	BLm+1	0V	+1V	0V	+1V	+5V
	BLm+2	0V	+1V	0V	+1V	0V
	BLm+3	0V	+1V	0V	+1V	+5V
Block 0 (selected)	BT1(0)	Vdd	Vdd	Vdd	Vdd	+10V
	WL0(0)	-15V	Versvfy	-15V	Vcorvfy	Vcorr
	WL1(0)	-15V	-4V	-15V	-4V	+2.5V
	WL31(0)	-15V	-4V	0V	-4V	+2.5V
	SL(0)	0V	0V	0V	0V	0V
	ST1(0)	Vdd	Vdd	Vdd	Vdd	0V
Block n (non-selected)	BT1(n)	0V	0V	0V	0V	0V
	WL0(n)	0V	0V	0V	0V	0V
	WL1(n)	0V	0V	0V	0V	0V
	WL31(n)	0V	0V	0V	0V	0V
	SL(n)	0V	0V	0V	0V	0V
	ST1(n)	0V	0V	0V	0V	0V

Note: * Ma, Mb, Mc and Md are selected
** Mi, Mj, Mk and Ml are selected
*** Mb and Md are correction inhibit
Ma and Mc are corrected

FIG. 11

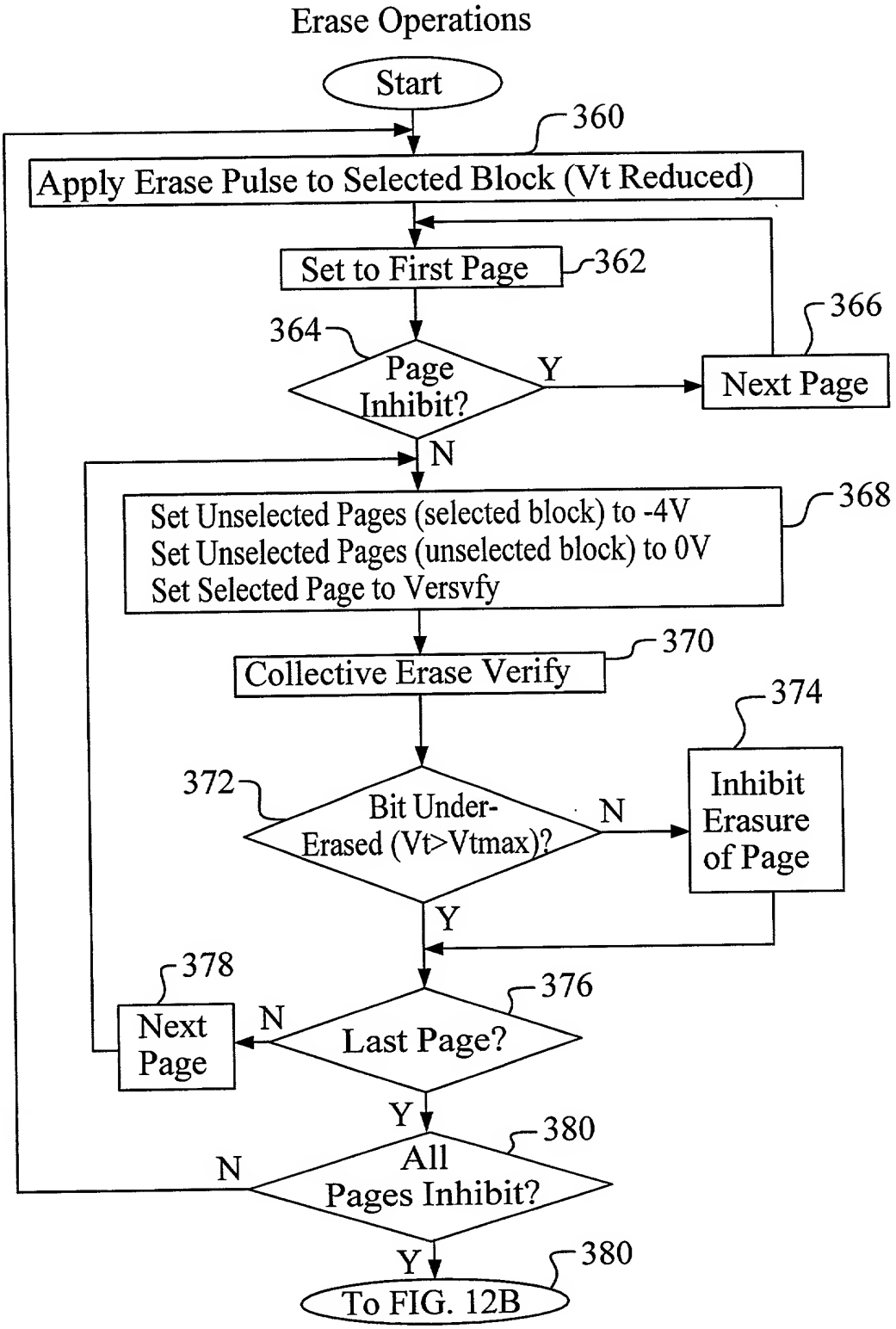
Erase Operations
Start
360
Apply Erase Pulse to Selected Block (Vt Reduced)
Set to First Page
362
364
Page Inhibit?
Y
366
Next Page
N
368
Set Unselected Pages (selected block) to -4V
Set Unselected Pages (unselected block) to 0V
Set Selected Page to Versvfy
370
Collective Erase Verify
374
372
Bit Under-Erased (Vt>Vtmax)?
N
Inhibit Erasure of Page
Y
378
376
Next Page
N
Last Page?
Y
380
All Pages Inhibit?
N
Y
380
To FIG. 12B

FIG. 12A

Correction Operations

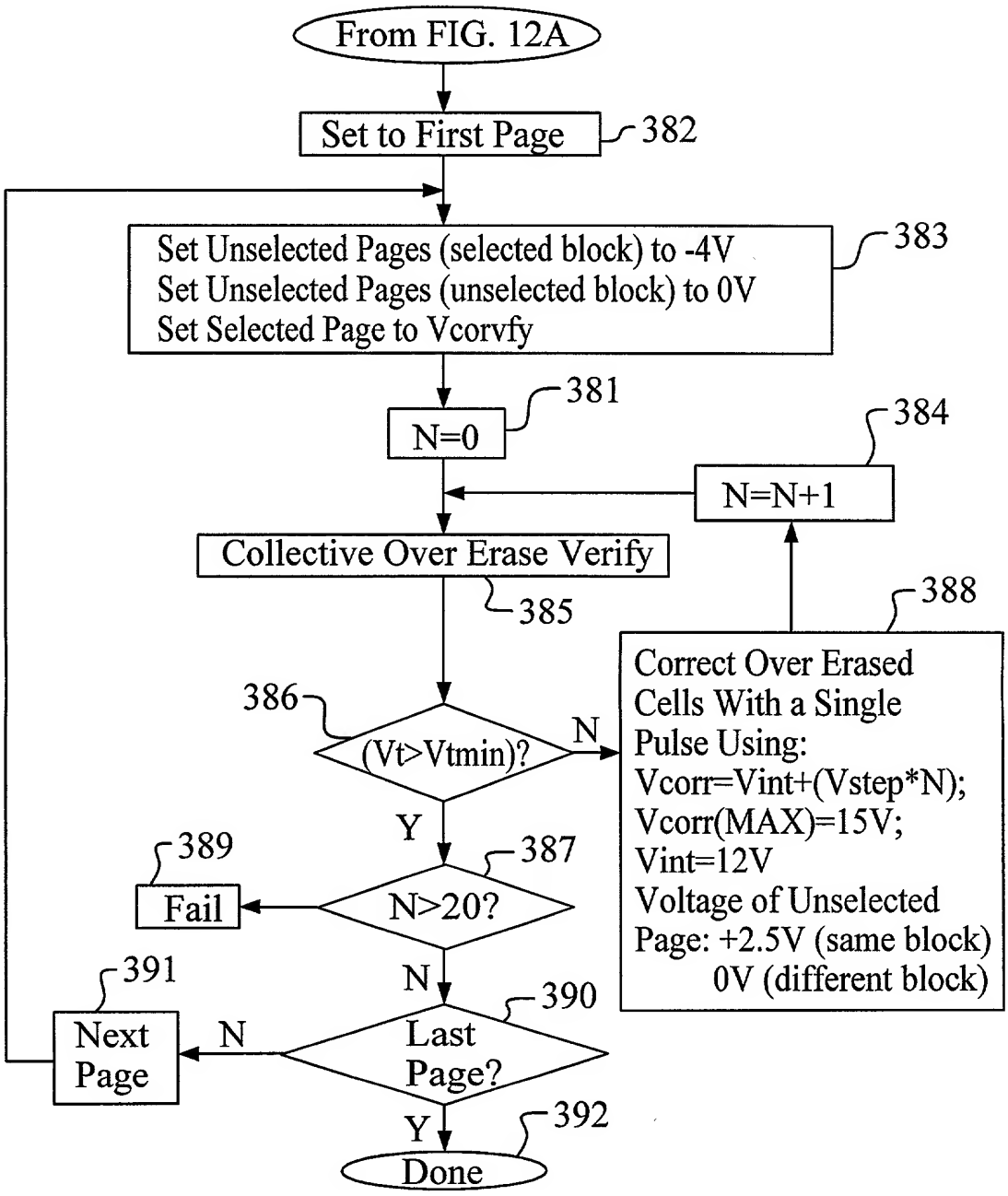

FIG. 12B